Design of a RFIC Hybrid for full-duplex communication on interconnects

By

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ABSTRACT

Transformer modeling and model parameter extraction is presented with a subsequent design of a Hybrid for full duplex communication using the extracted model. ASITIC is used to extract the S-parameters from a planar transformer in TMSC CMOS 0.35 μm process between 1GHz and 20 GHz. Genetic Algorithm in MATLAB is used to find the model circuit values so to get the best fit of the S-parameters obtained from ASITIC to the ones of the model such that the model could be used in SPICE. Furthermore, exhaustively, many transformers are autonomously generated, their S-parameters extracted and the transformer parameters that give the best performance are found. Cadence is used to simulate two hybrid circuits based on the extracted transformer model. The results of the simulations at 10Gbps show a full-duplex operation with good isolation of around 40 dB but with relatively high losses of 10dB with respect to the ideal case (16dB total). The resultant received to transmit peak voltage ratio is found to be 0.15 with a 6dB pulse width of 10 ps.

ACKNOWLEDGEMENTS

I would like to thank my supervisor, Professor Tony Chan Carusone, for all the help and inspiration he provided during my studies and during my thesis work. In addition, I would like to thank my parents for inspiring me to pursue a career in electrical engineering. I would also like to thank Engineering Science office staff, Louisa Muzzin and Morag Paton for timely and kind responses to my inquires.

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1. INRODUCTION

Full duplex communications is an efficient way to double the bandwidth of a wire-line channel. To be able to transmit and receive at the same time we need to somehow subtract the transmitted signal from the received signal. This can also be thought of as having two electromagnetic waves traveling in opposite directions without any interference and subtracting each other when they meet. Therefore we can borrow the ideas on how to implement this type of device from the microwave domain. In microwave engineering there is a class of devices called Hybrids and Couplers that allow isolation between some ports through connections between others. The basic idea is that the waves travel inside of the device in several paths such that when they combine at some points the wave destructively interfere, this is what happens at the isolated port. There also places where the waves constructively combine, this happens at the through port. The waves are the TEM waves, and can be represented in terms of voltages and currents, thus circuit gives the same complete description as the one with waves.

A hybrid is usually implemented using electrically long wires such that destructive or constructive interference can be created. Another way to do it is to use lumped elements to introduce the necessary phase shifts. The subject of this thesis is to design a lumped element hybrid in CMOS process using planar transformers. To do this we need to have a good model that describes well the relevant Electromagnetic phenomena.

2. PLANAR TRANSFORMER MODELING

2.1 Overview

Planar solid state inductors and transformers are widely used in transistor biasing networks, VCO's, baluns (balanced/unbalanced line converters), lumped-element hybrids, couplers and phase shifters. In the majority of the applications the bandwidth of operation of inductors and transformers has to be as wide as possible. This is especially true in spread spectrum modulation schemes and in digital communication. Therefore, it is important to develop accurate wide-band models of inductors and transformers so that the system-level behavior can be accurately predicted. Relatively small number of papers is written on the subject of inductor and transformer modeling. It is a common misconception that the wide-band behavior is well understood.

2.2 Transformer models

Two common wideband transformer models reported in literature are shown below:

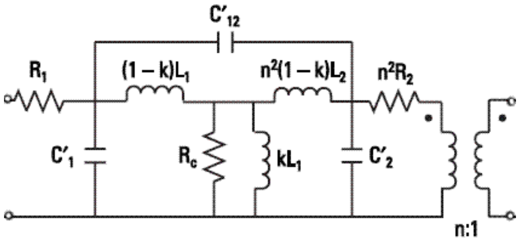

Figure 1. Transformer model reported by I. J. Bahl [5]

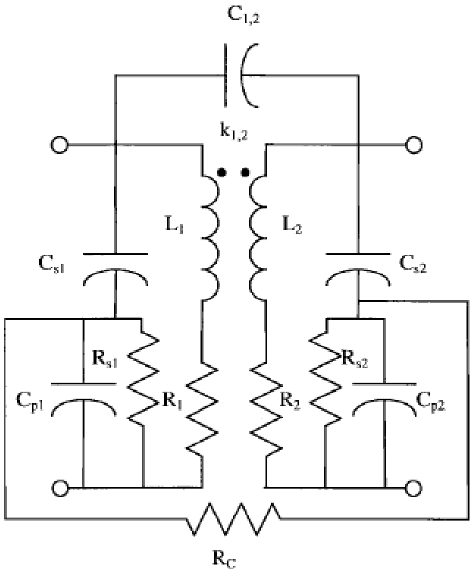

Figure 2. Transformer model reported by A. M. Niknejad [6]

The first circuit (see Figure 1) models the wideband behavior of a planar transformer. The model consists of an ideal transformer to the right and a loss network to the left. The loss network models the following phenomena: capacitive (C_{12}) and inductive (kL_1)

coupling between the windings, inductance leakage ($(1-k)L_{1,2}$) of the winding, capacitance ($C_{1,2}$) of the windings (which also models the skin effect losses), DC losses in the windings (R_1, R_2), and a DC loss of the core (R_C) which could act as a frequency independent approximation for the eddy current loss. One important disadvantage of this model is that it is not symmetrical with respect to the ports. The second disadvantage of this model is that eddy current loss modeling is not frequency dependent, which is far from true at high frequencies.

A better wideband transformer model reported by A. M. Niknejad (see Figure 2) describes the following phenomena: DC and AC (skin effect) losses in wires, capacitive and inductive coupling between the windings, resistive coupling through the substrate, and the eddy current loss in the substrate. The transformer symmetry is preserved in this model as opposed to the previous one. In many applications the transformer layout is symmetrical, that is the turn ratio is 1:1. Thus the windings can be interchanged without any effect. To simplify the model the symmetry can be exploited by equating the symmetrical components of the model (true only for 1:1 turn ratio).

2.3 Extraction of the S-Parameters

To get a wideband model for a particular transformer it is necessary to characterize the transformer using S-, Z- or ABCD- parameters. In most cases a 2-port differential model is sufficient. There is practically no new information gained by looking at the 4-port model. By extracting the port parameters at different frequencies it is possible to make them fit the ones of a particular lumped element model, for example the one on Figure 2. This method fails if the model inadequately predicts the wideband behavior of the transformer, or when the assumption about the port symmetry is invalid.

For the purposes of this thesis, it is important to extract a circuit that correctly models the wideband behavior of a transformer. The first step is to extract the port parameters, and the second step is to fit the circuit model to these parameters. At a later stage this circuit model will be used to design and simulate a Hybrid circuit in SPICE.

The S-parameters are extracted with ASITIC[1] using *2PortTrans* command for 1 GHz – 20 GHz frequency range, with eddy option turned on to include eddy current calculation. ASTIC uses a technology file that describes the semiconductor layers: their dimensions and conductivities. The technology file is set up from the datasheets for TSMC 0.35 μm CMOS process, with chip size set to 300 μm x 300 μm to reduce the computation time. For the technology file the FFT size is set to 1024x1024 so that the smallest size of around 0.3 μm can be modeled correctly during the mesh generation. The FFT size has a significant effect on the amount of the hard disk space used. For this case a data file of 340 MB is created by ASITIC for a single frequency point. The file contains precomputed data for FFT that significantly speeds up the computation.

A coil with the following near-optimal parameters is used:

Parameter Abbreviation	**Description**	**Value**
N	Number of turns	4
L	Side length	150 μm
W	Winding width	5 μm
S	Inter-winding spacing	0.3 μm
	Metal layer	top
	Grounding structure size	1 μm^2

Table 1. ASITIC transformer parameters

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[1] ASITIC (Analysis and Simulation of Spiral Inductors and Transformers for ICs) freely available at: http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

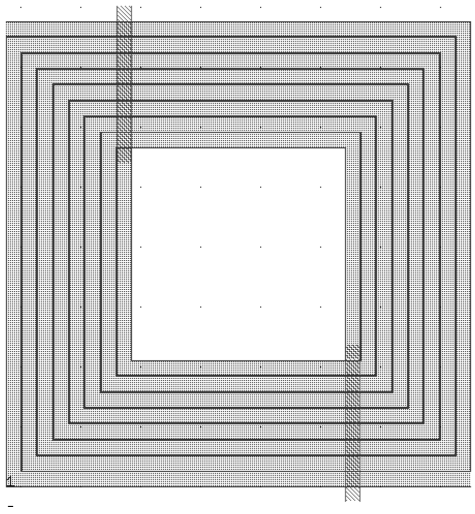
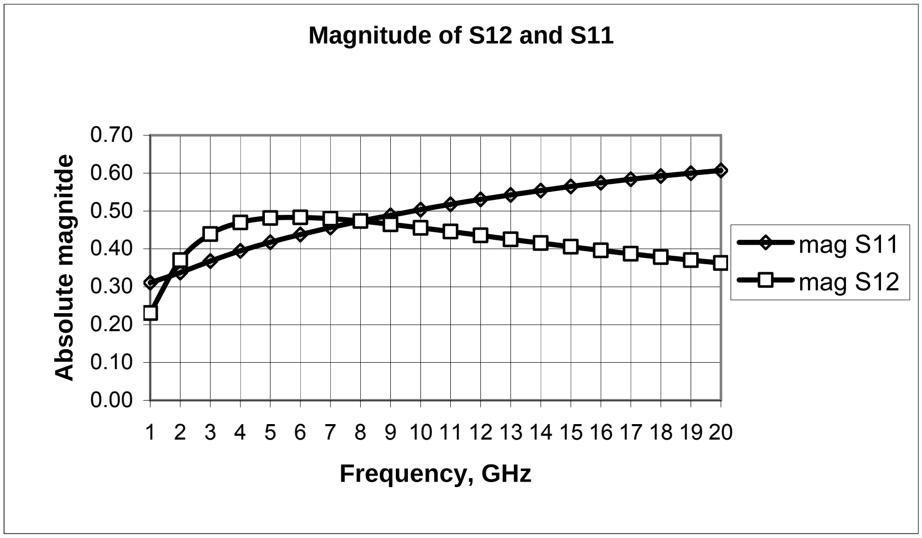


Figure 3. ASTIC transformer layout.
L=150 µm, W=10 µm, S=0.3 µm, N=4

The S-parameters are extracted using ASITIC between 1GHz and 20GHz at 20 points, as shown on the graphs below:



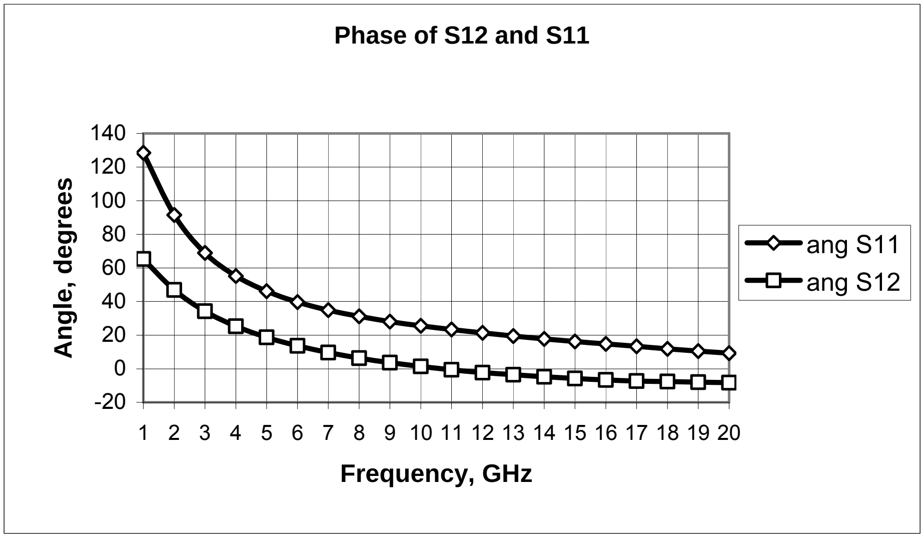


Figure 4. Magnitude and phase of the extracted S-parameters. Due to symmetry, S22 & S21 are the same as S11 & S12 respectively and, thus, are not shown

2.4 Model extraction from the S-Parameters

To extract the circuit model from the S-parameters the following steps are taken:

1. Generate two SPICE netlists for the circuit on Figure 1, with short and open circuited secondary winding and a voltage source at primary winding.
2. Use SCAM[2] to symbolically calculate all the nodal voltages & currents for the circuit on Figure 1, using symbolic names of the circuit elements, instead of values.
3. Get a symbolic expression of ABCD-parameters using the following equations [1]:

$$A=\frac{V_1}{V_{2,oc}};B=\frac{V_1}{I_{2,sc}};C=\frac{I_{1,when V_1 \, is\, applied}}{V_{2,oc}};D=\frac{I_{1,when V_1 \, is\, applied}}{I_{2,sc}}$$

   ABCD-parameters are used instead of Z- and S- parameters for two reasons: easier cascading, and simpler expression in terms of voltages & currents (these expressions take several pages).

4. Print these general expressions in MATLAB and insert them into a MATLAB routine that calculates ABCD parameters for the given values of the circuit components (Figure 2).
5. Use MATLAB to convert ABCD-parameters to S-parameters at each vector of circuit values. See [1] for conversion formulas.

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[2] SCAM (Symbolic Circuit Analysis in MATLAB) using MATLAB symbolic toolkit, freely available at: http://www.swarthmore.edu/NatSci/echeeve1/Ref/mna/MNA6.html

6. Use Genetic Algorithm (GA) to find the circuit values that give the smallest RMS error when fitting the S-parameters of the model (from step 4) to the ones from ASITIC. If “Genetic Algorithm & Optimization” toolkit is available then it is recommended over manual coding of GA.

2.5 Genetic Algorithm based curve fitting

GA based curve fitting and optimization is a very versatile compared to other methods, such as LMS and other gradient descent methods [2]. GA is especially powerful in highly nonlinear, noisy, multidimensional environments. GA, unlike the other methods, is guaranteed to eventually find an optimal minimum. Main disadvantages of GA are its bigger memory requirements and slower speed of convergence, although it can be made faster if implemented on a parallel computer.

Genetic Algorithm works in a similar way as natural selection. GA operates on a set of individuals, called population, where each individual is a vector of numbers (like DNA), that completely defines it. GA starts with a set of vectors with random values (chosen from some distribution) with vector size determined by the problem. For example in this project there are 8 numbers in a vector, representing a value of each circuit element (assuming symmetry we do not need the rest). GA then proceeds to perform four particular operations for many iterations. For each iteration the following four operations are performed: cross-breeding, error calculation, finding the best individual, and mutation.

Cross-breeding: randomly pick two individuals (parents) to create another individual (child) with a vector of parameter values derived from the parents (for example. by averaging the two vectors).

Error calculation: calculating the error (1/fitness) value for each individual called. For S-parameter curve fitting this can be done by calculating the RMS error between the actual and individual’s S-parameters. Where individual’s S-parameters are calculated for a given circuit defined by the individual’s parameter vector. In this project, the error is calculated as a sum of squared differences between the four S-parameters (S11, S12, S21, S22). This takes into account that S-parameters are complex in general and thus squaring the difference will lead to fitting both magnitude and phase plots. In future the weighting may be applied in error calculation for the different S-parameters (for example when S12 is more important than S11).

Finding the best individual: Sorting the population in order of its error

Mutation: Picking individuals at random with a small probability, and adding small noise to the parameter vector. This is a main mechanism by which GA eventually finds individual with the smallest error.

By executing the above operations for many iterations the algorithm finds better and better parameter vector as time progresses. Eventually an absolute minimum of error is found and the best circuit parameters are inserted into SPICE. The graphs (Figure 5, 6) below illustrate the accuracy of fitting and validation of the model in Agilent ADS. The following transformer parameters were chosen by optimization (see next section):
Side Length=200 μm, Width=10 μm, winding Separation=0.3 μm, N=3 turns

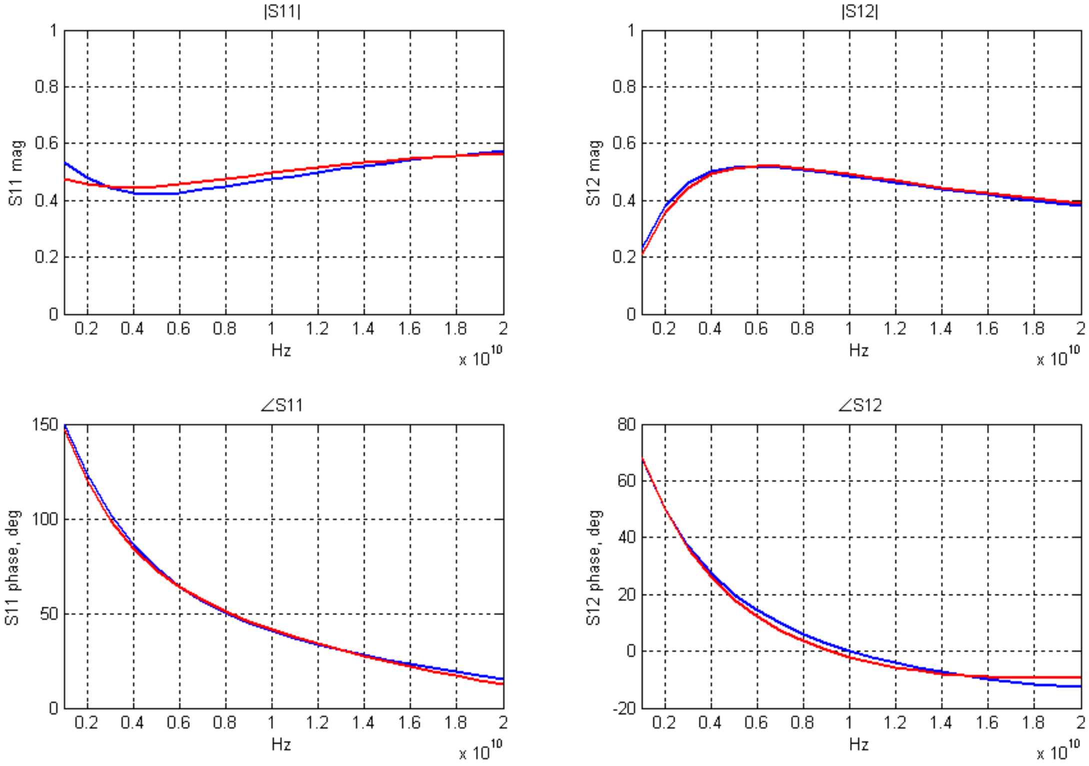

Figure 5. ASITIC and GA fitted S-parameters.
Red: GA fitted, Blue: from ASITIC

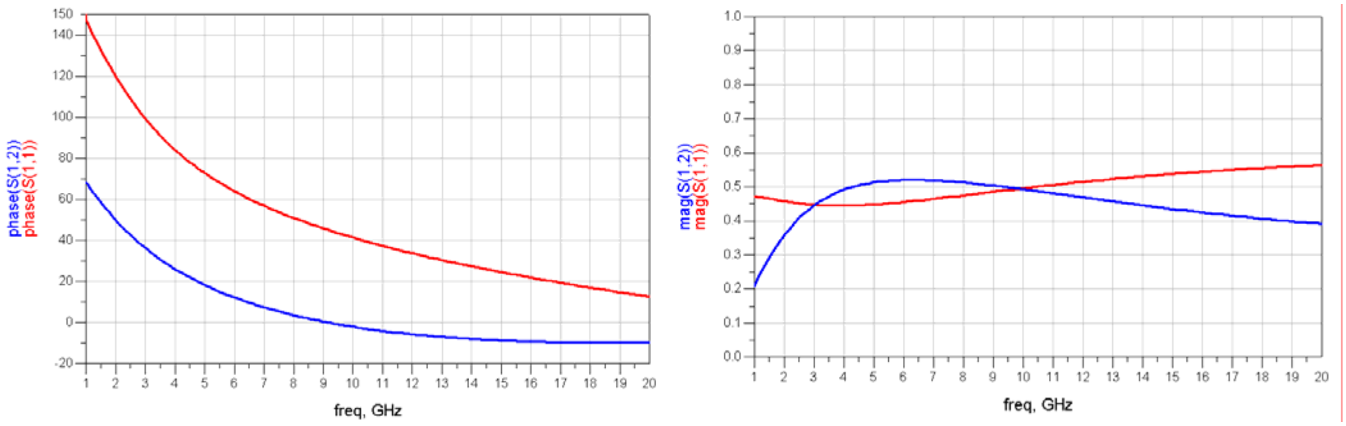

Figure 6. S-parameter curves obtained in ADS from the GA-derived circuit model

The following values are extracted using GA (refer to Figure 2, or Figure A1):

Circuit element	Value
C 1,2	21.9 fF
L 1, 2	0.472 nH
k	0.776
Cs 1, 2	17.4 pF
Cp 1, 2	11.8 fF
R 1, 2	17.7 Ω
Rs 1, 2	1.8 KΩ
Rc	133.1 Ω

Table 2. GA - extracted circuit parameters

2.6 Transformer optimization

In order to improve performance of the whole system it is important to optimize the parameters of the transformer, such as the surface area, number of turns, line width, and spacing. Exhaustive S-parameter evaluation with ASITIC is done for various values of the transformer parameters. The obtained S-parameter graphs can be found in the appendix (Figures A2, A3, A4, A5). The transformer performance criteria, in order of decreasing importance, are chosen to be: the coupling factor, bandwidth (high frequency roll-off), high inductance, smaller S11 (depends on losses and S21). There are many other techniques to optimize transformer performance, such as stacking [3], higher order polygonal geometries, oxide removal, parallelizing coils to reduce skin effect resistance, and others which are not considered here. It also should be noted that the effect of ground plane on the S-parameters is minimal in the case of 0.35 μm CMOS process, although it tends to slightly increase losses due to the eddy currents [8].

2.7 Summary

The transformer model is extracted and the values of the circuit elements are found using the Genetic Algorithm. The GA-based approach yields a very good model that produces S-parameters that are very close to the ones obtained from ASITIC. The small discrepancies in GA fitting (Figure 5) could be caused by: asymmetry in ports, insufficient GA convergence time and inefficient weighting when calculating error in GA algorithm.

3. DESIGN OF A HYBRID

3.1 Overview

Hybrids are used in many applications, such as telephony, amplifiers, RF receivers and transmitters, and practically anywhere there is a need for isolation between a receiver and a transmitter. Typically, hybrids are four-port devices with Input port, Through and Coupled outputs, and an Isolated port. Coupled port, unlike through port, is usually electrically (capacitively or inductively) separated from the input. Ideally, the isolated port has zero voltage no matter what the input voltage is. If one were to switch input and isolated ports, that is, apply power to the isolated port, then one would find that there would be no power at the input port. This means that there is symmetry between the input and the isolated ports. This symmetry is exploited such that one can transmit from the input port to the coupled port (or through port) and receive on the isolated port only what comes from the coupled port (assuming through port is terminated in Z_0). The following diagram illustrates a general setup for isolating a receiver and a transmitter:

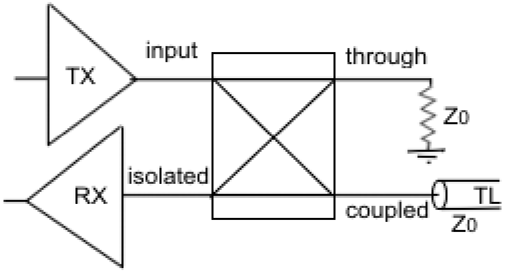

Figure 7. A general setup for driving a hybrid
to achieve full-duplex operation

3.2 Design specifications

Before designing the hybrid it is necessary to set up the performance criteria sought. The two main criteria are: the isolation and loss. The degree of isolation specifies how much power is coupled from the input port to the isolated port when the other ports are terminated in Z_0. Loss is another important factor, it tells how much power is lost from input port to the output port (coupled or through). Loss is usually different when the transmission line is connected at coupled or through port. This is due to the different frequency dependence of the transfer characteristics between ports, since input-to-coupled characteristic is high pass and input-to-through a lowpass. The following sections will introduce two common hybrid designs

3.3 Design comparison

There are many various hybrid circuits. There are designs [4], [5], [7] that model the microstrip couplers with lumped elements by breaking down the transmission lines into equivalent periodic structures. But they usually use capacitors which are usually much bulkier. Designs discussed here do not use capacitors, only inductors and 50 Ω resistors. The following two main designs of a hybrid are considered based on the references 4 and 5.

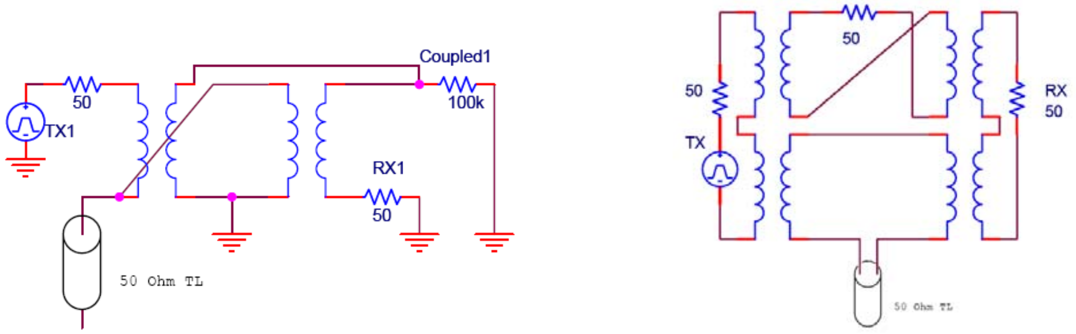

Figure 8. Schematics of two hybrids [5] left, [4] right.
In both cases each transformer is represented by the extracted transformer model.

As we see from the above figure the hybrid to the right uses four 2-winding transformers or alternatively two 3-winding transformers (baluns), the advantage is clear.

The following frequency performance is extracted with, and without, artificially added bypass capacitors so as to make the model perform correctly around 40GHz. This behavior is outside of the one being extract from ASITIC (1-10GHz) and is most probably not realistic (it will be attenuated by the transmission line in as similar low pass manner).

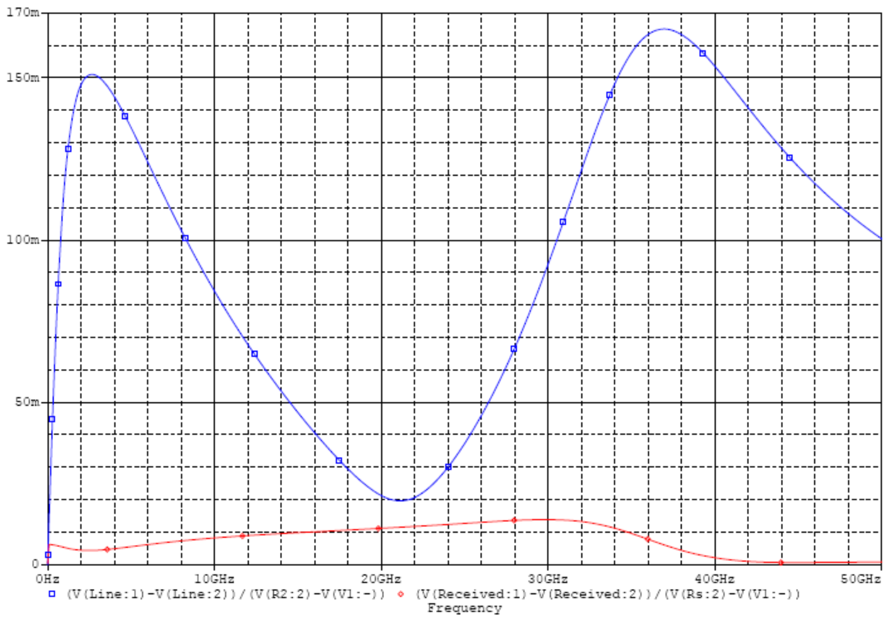

Figure 9. Frequency response of the hybrid without bypass capacitors (linear scale)

Red: received signal, Blue: signal delivered to the transmission line.

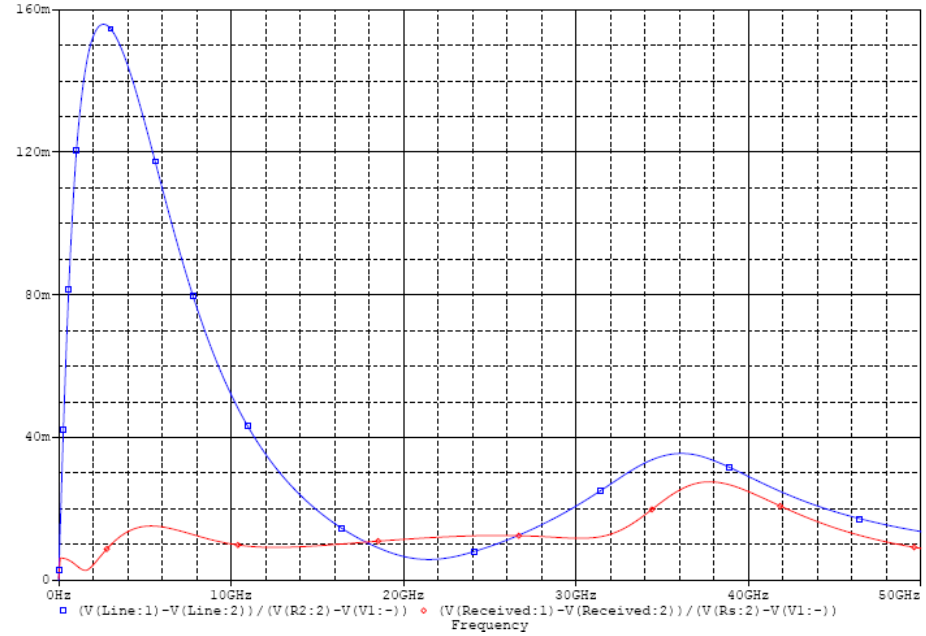

Figure 10. Frequency response of the hybrid with bypass capacitors (linear scale)

A step response is also extracted below.

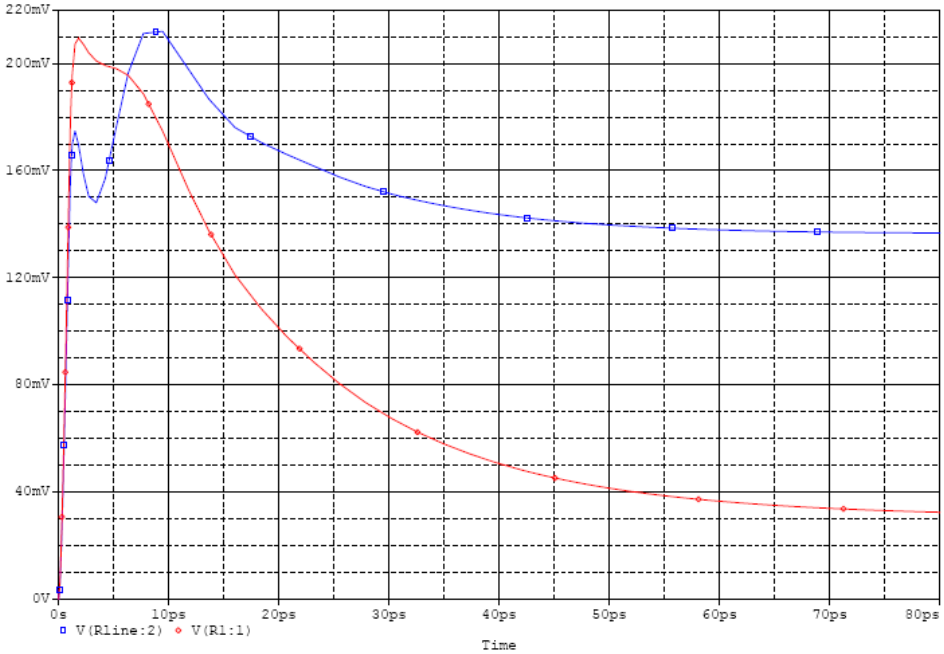

Figure 11. Step response of the hybrid (step is applied at the transmitter end).

Red: coupled signal, Blue: though signal, delivered to the transmission line

3.4 Final design simulation

To test the full-duplex operation of the hybrid-based interconnection a test is performed where two rectangular waveforms are transmitted simultaneously at 10Gbps. The waveforms are chosen to be 1001 and 0101 (where 1 is 1V and 0 is 0V).This particular selection attempts to reveal interference effects during the simultaneous transmission, and the isolation between the transmitter and the receiver for both sides. The hybrid-based interconnection is implemented using the hybrid circuit of Figure 8 (rleft) with a transformer model with values in Table 2 (section 2.5). The interconnection between the hybrids is accomplished through a 20 cm, lossy transmission line (for detailed parameters see Figure A6 in appendix). The following diagram illustrates the setup:

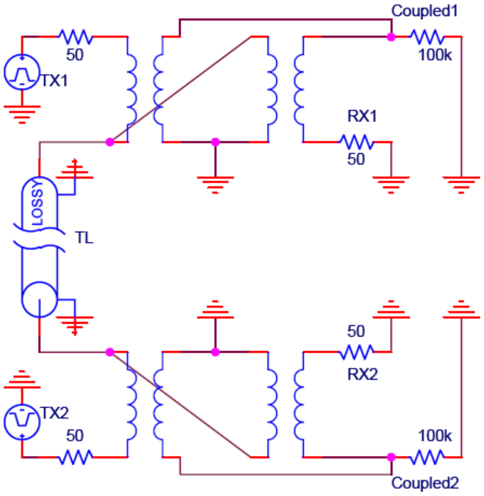

Figure 12. Cadence Capture schematic of the setup used to investigate the full-duplex operation

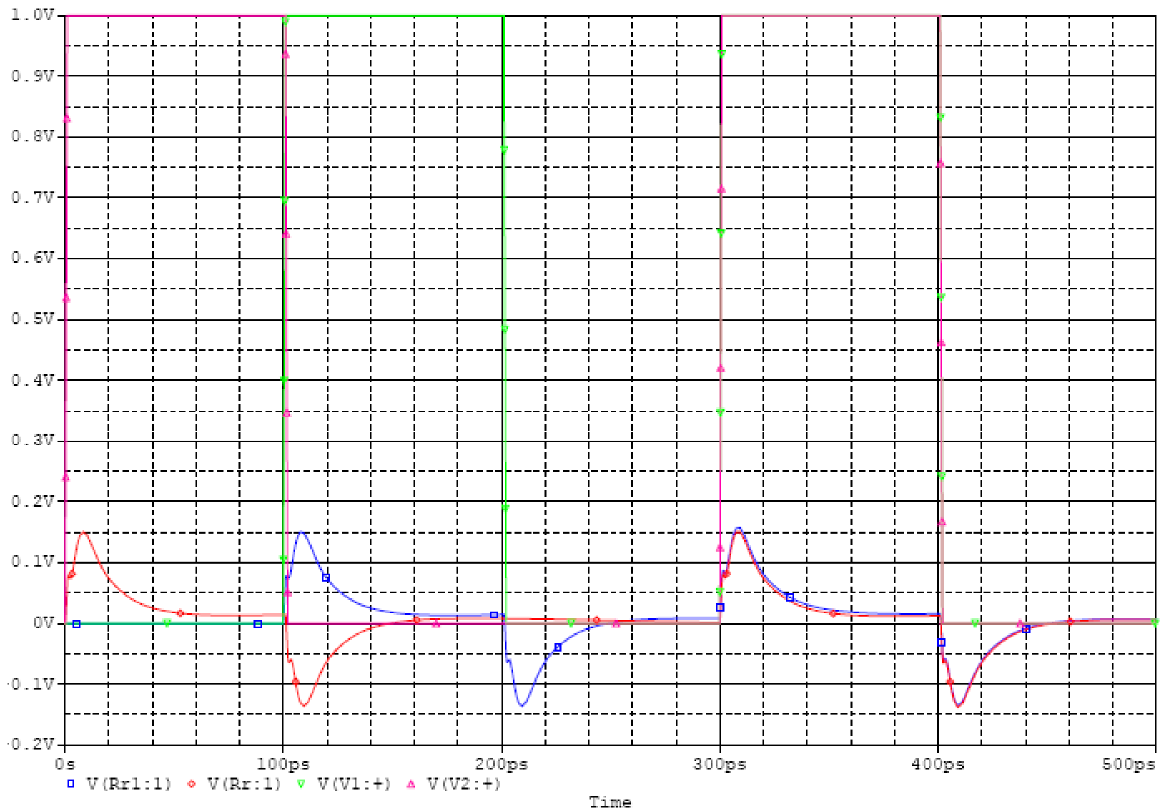

Figure 13. SPICE simulation of a circuit on Figure 12 with circuit values on Figure A6 in appendix. The rectangular waveforms corresponding to 1001 and 0101 are send both ways and the received signals are observed at both ends. The small decaying peaks represent received signals (red: first receiver, blue: second one)

The results of simulations show that the isolation is very good (around 30dB), when one of the transmitters send the signal the receiver on the same end does not detect anything. The loss, voltage ratio between the transmitter and the receiver on the other end, is relatively high. From a pulse of 1V the received voltage is 150mV. Another important characteristic is pulse-width, which in this case is very good. Pulse width, measured between halves of max voltage, is found to be around 10 ps, which provides plenty of time for the tail to die down before the next symbol is transmitted.

3.5 Summary

The hybrid circuit was simulated using a model extracted from ASITIC and Genetic Algorithm. The hybrid performance is quite adequate, although there are quite a lot of losses. The total loss in the link between the chips is 16 dB or 10dB more than the expected 6dB (for the maximum power transfer). The pulse-width was found to be around 10ps which is very good. One major problem is that the through port was used and a small DC voltage offset propagated to the receiver (see Figure 13).

4. CONCLUSIONS

4.1 Summary

The modeling of the planar transformer is conducted and the wideband circuit model is extracted using Genetic Algorithm and ASITIC. Furthermore, the model is used to design and simulate a hybrid circuit in SPICE. The performance of the hybrid in a interconnection of two devices at 10Gbps is found to be satisfactory. The loss was found to be around 16dB and isolation around 30dB for the full 2-device setup. The intersymbol interference is observed to be very minimal due to a fast tail off of the step response of the hybrid. It is hypothesized that the system could operate beyond the designed 10Gbps.

4.2 Future work

For transformer design several improvements can be made. Firstly, octagonal shape should be used to increase the inductance and reduce fringing capacitance at the corners [8]. Secondly, parallel stacking should be used to reduce the surface area and also capacitive coupling to the substrate [3]. Thirdly, Agilent Momentum should be used to get more realistic S-parameters.

For hybrid circuit, planar capacitors might be added to the circuit so as to increase the coupling and thus reduce the insertion loss. A complete hybrid simulation needs to be performed in ADS, ASITIC or Momentum. This is important, because inter transformer coupling is not modeled, nor are the resistors or wires. Another possible improvement is to incorporate active devices into the hybrid as it is done in [9]. Where transistors are used to compensate for the losses and increases bandwidth of the hybrid.

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APPENDIX

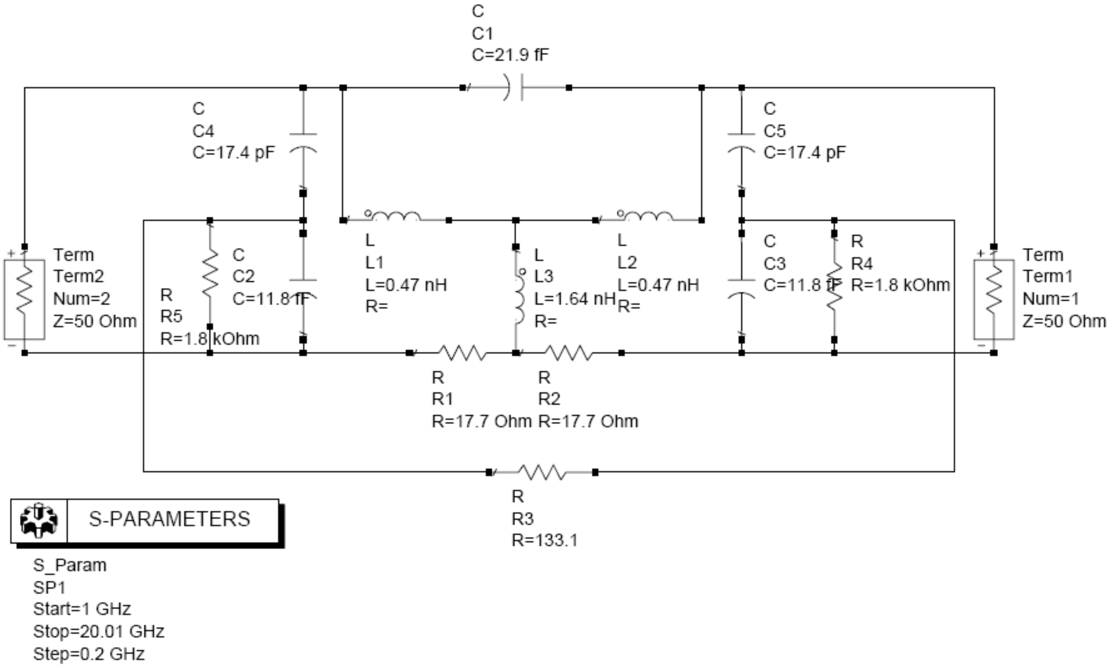

Figure A1. ADS circuit for Figure 6, section 2.5.
Circuit values were derived using GA algorithm

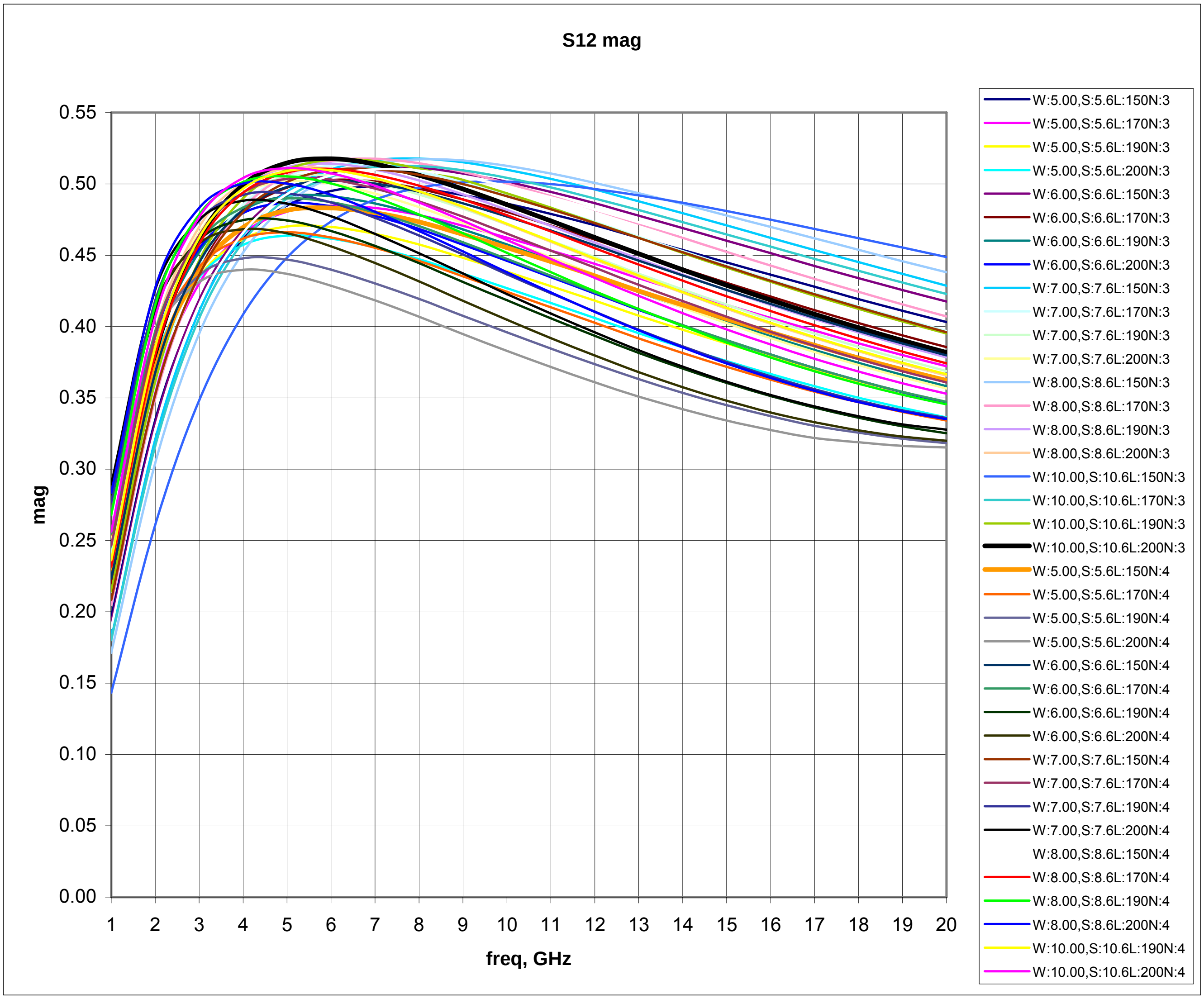

Figure A2. Transformer optimization. S12 magnitude

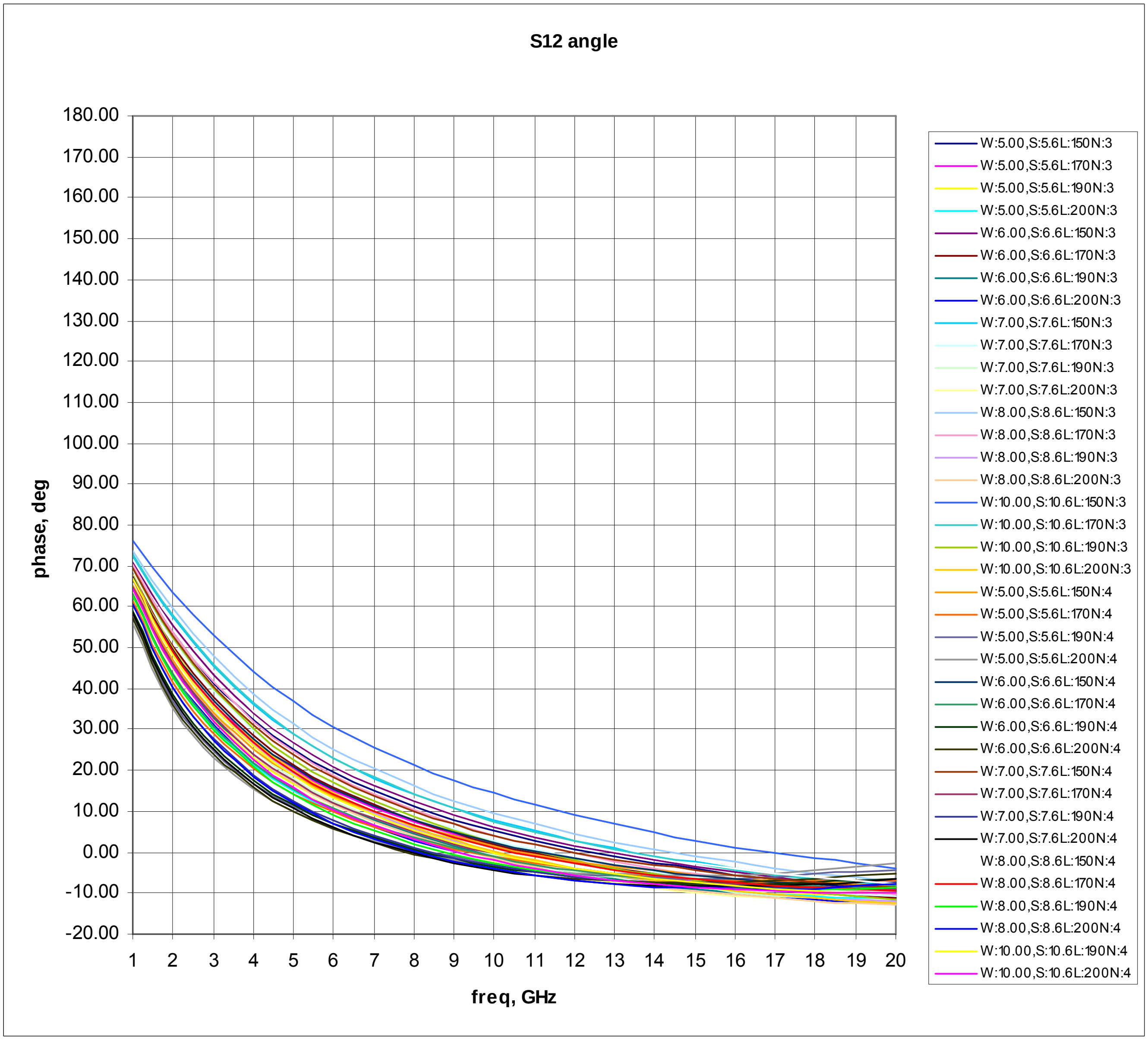

Figure A3. Transformer optimization. S12 phase

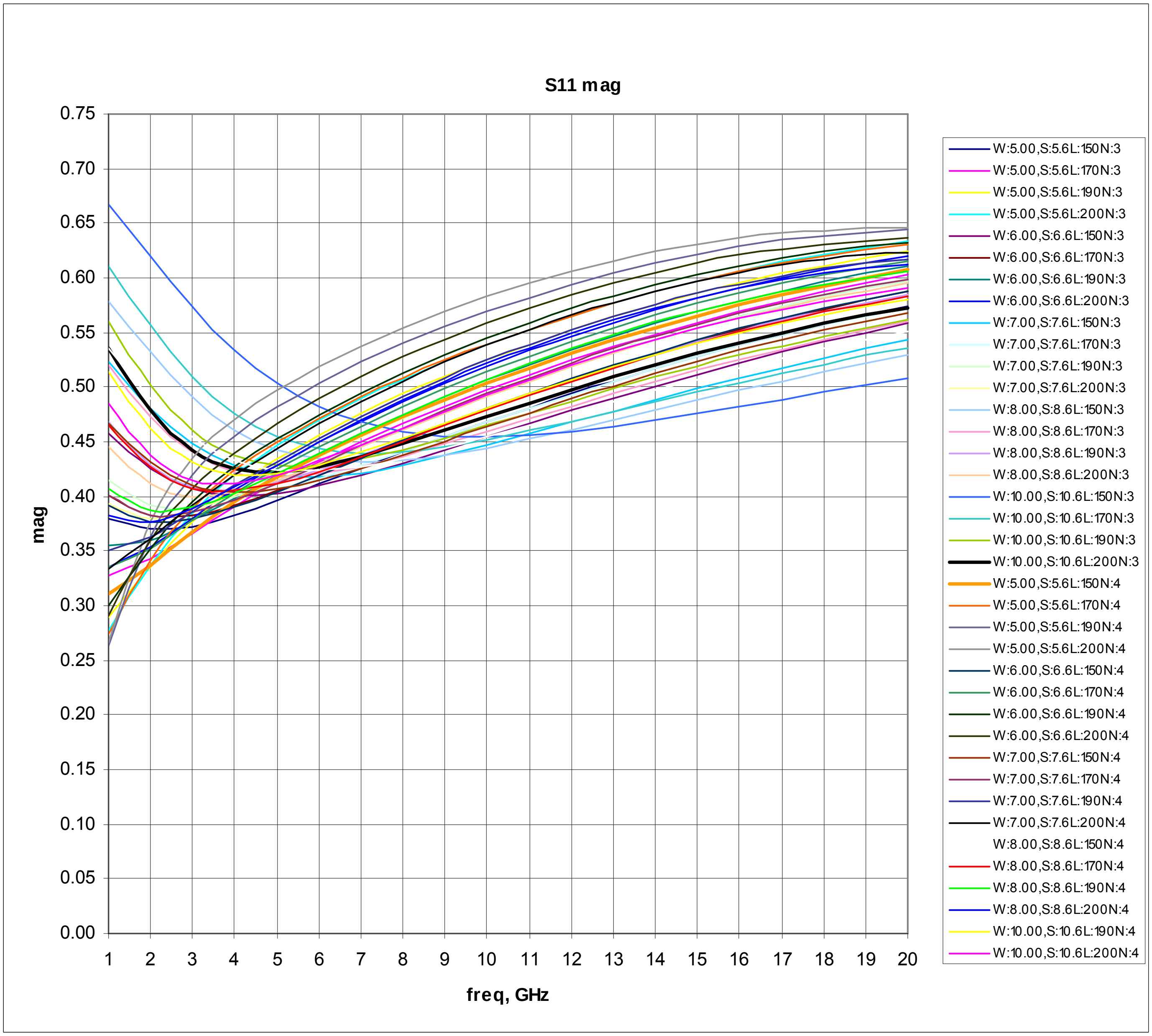

Figure A4. Transformer optimization. S11 magnitude

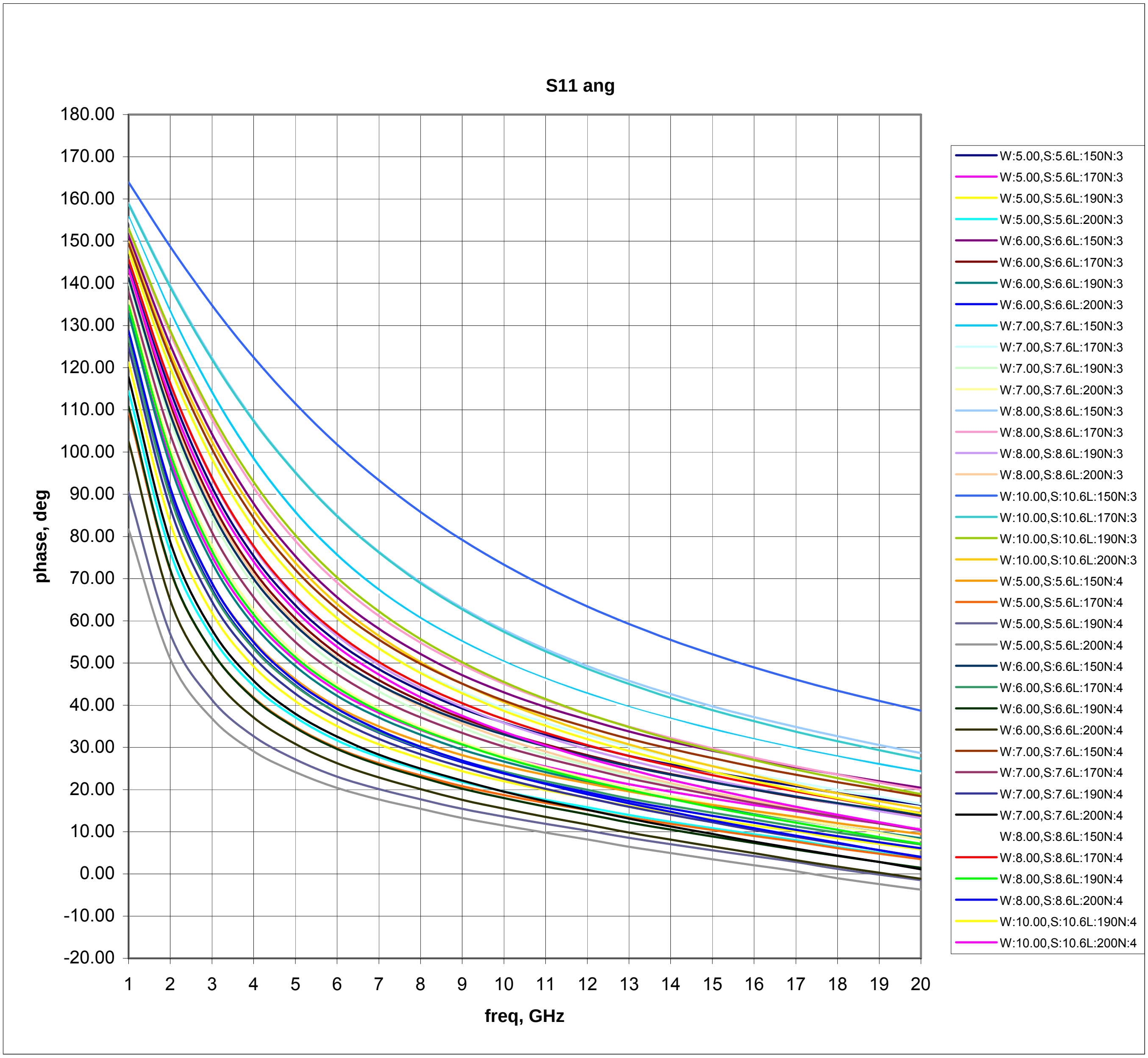

Figure A5. Transformer optimization. S11 phase

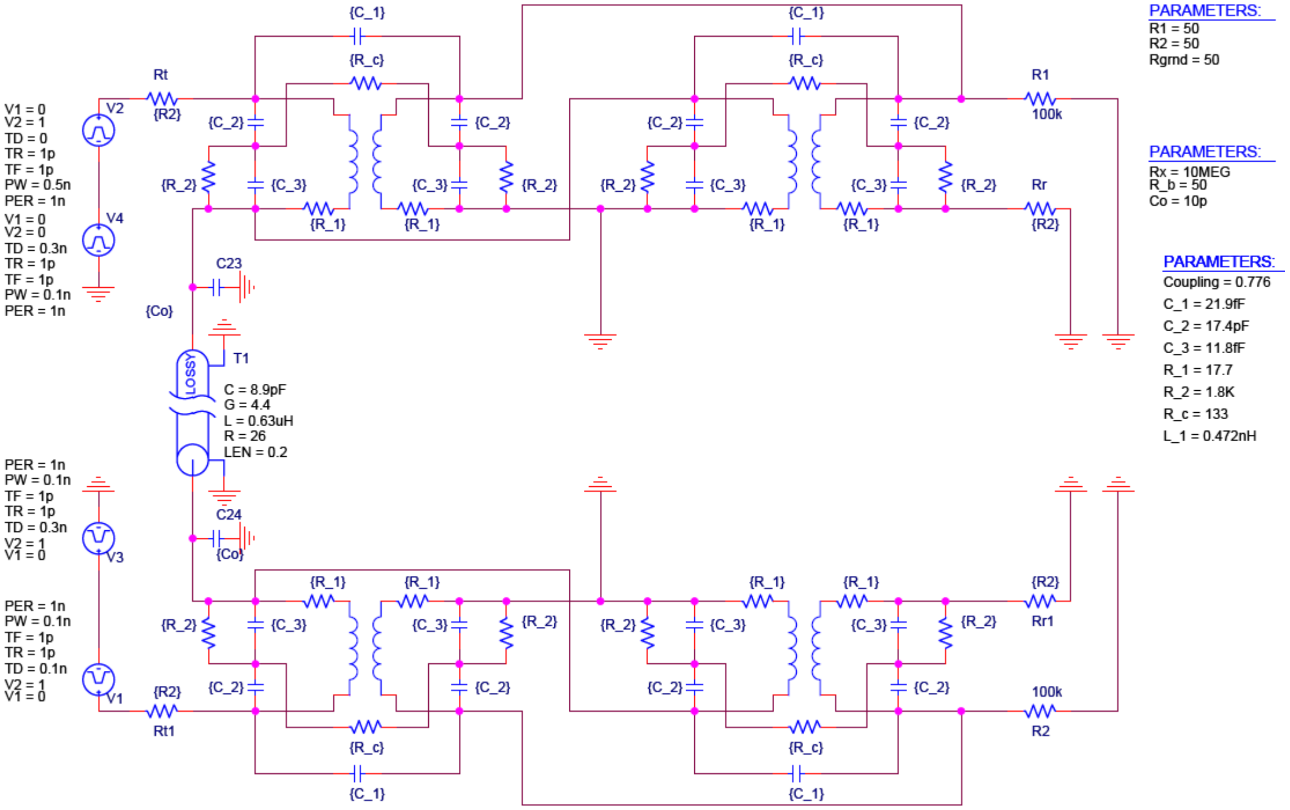

Figure A6. Cadence Capture schematic for testing simultaneous transmission and reception of a test sequence. Capacitors are inserted before and after the transmission line to combat reflections.